FIG. 1A

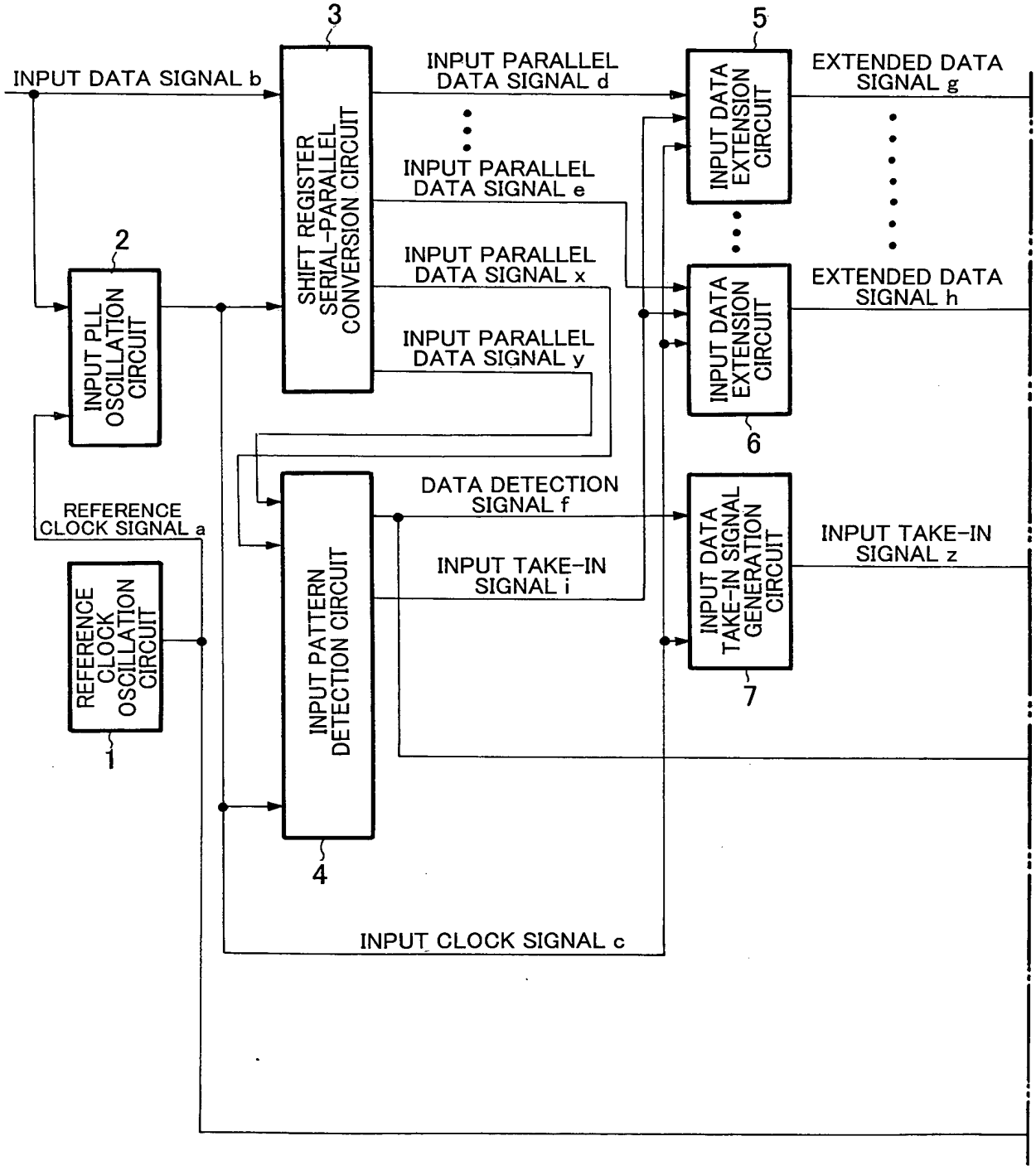

3
5
INPUT DATA SIGNAL b
SHIFT REGISTER SERIAL-PARALLEL CONVERSION CIRCUIT
INPUT PARALLEL DATA SIGNAL d
INPUT PARALLEL DATA SIGNAL e
INPUT PARALLEL DATA SIGNAL x
INPUT PARALLEL DATA SIGNAL y
INPUT DATA EXTENSION CIRCUIT
EXTENDED DATA SIGNAL g
EXTENDED DATA SIGNAL h
2
INPUT PLL OSCILLATION CIRCUIT
6
REFERENCE CLOCK SIGNAL a
DATA DETECTION SIGNAL f
INPUT TAKE-IN SIGNAL i
INPUT DATA TAKE-IN SIGNAL GENERATION CIRCUIT
INPUT TAKE-IN SIGNAL z
7
REFERENCE CLOCK OSCILLATION CIRCUIT
1
INPUT PATTERN DETECTION CIRCUIT
4
INPUT CLOCK SIGNAL c

FIG. 1B

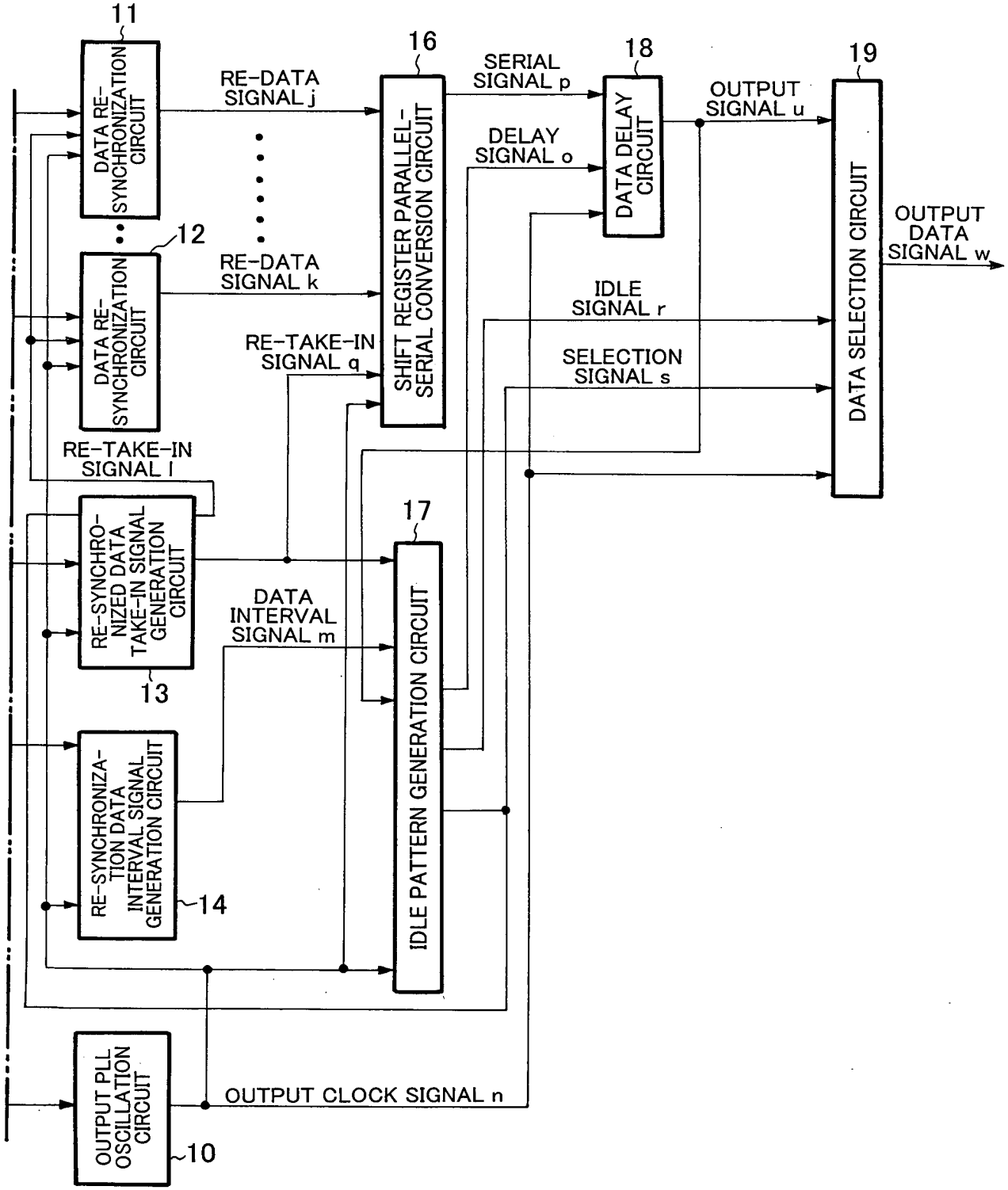

11
DATA RE-SYNCHRONIZATION CIRCUIT
12
DATA RE-SYNCHRONIZATION CIRCUIT
RE-DATA SIGNAL j
RE-DATA SIGNAL k
16
SHIFT REGISTER PARALLEL-SERIAL CONVERSION CIRCUIT
SERIAL SIGNAL p
DELAY SIGNAL o
18
DATA DELAY CIRCUIT
OUTPUT SIGNAL u
19
DATA SELECTION CIRCUIT
OUTPUT DATA SIGNAL w
IDLE SIGNAL r
SELECTION SIGNAL s
RE-TAKE-IN SIGNAL q
RE-TAKE-IN SIGNAL l
RE-SYNCHRONIZED DATA TAKE-IN SIGNAL GENERATION CIRCUIT
13
17
IDLE PATTERN GENERATION CIRCUIT
DATA INTERVAL SIGNAL m
RE-SYNCHRONIZATION DATA INTERVAL SIGNAL GENERATION CIRCUIT
14
OUTPUT PLL OSCILLATION CIRCUIT
10
OUTPUT CLOCK SIGNAL n

FIG.2A

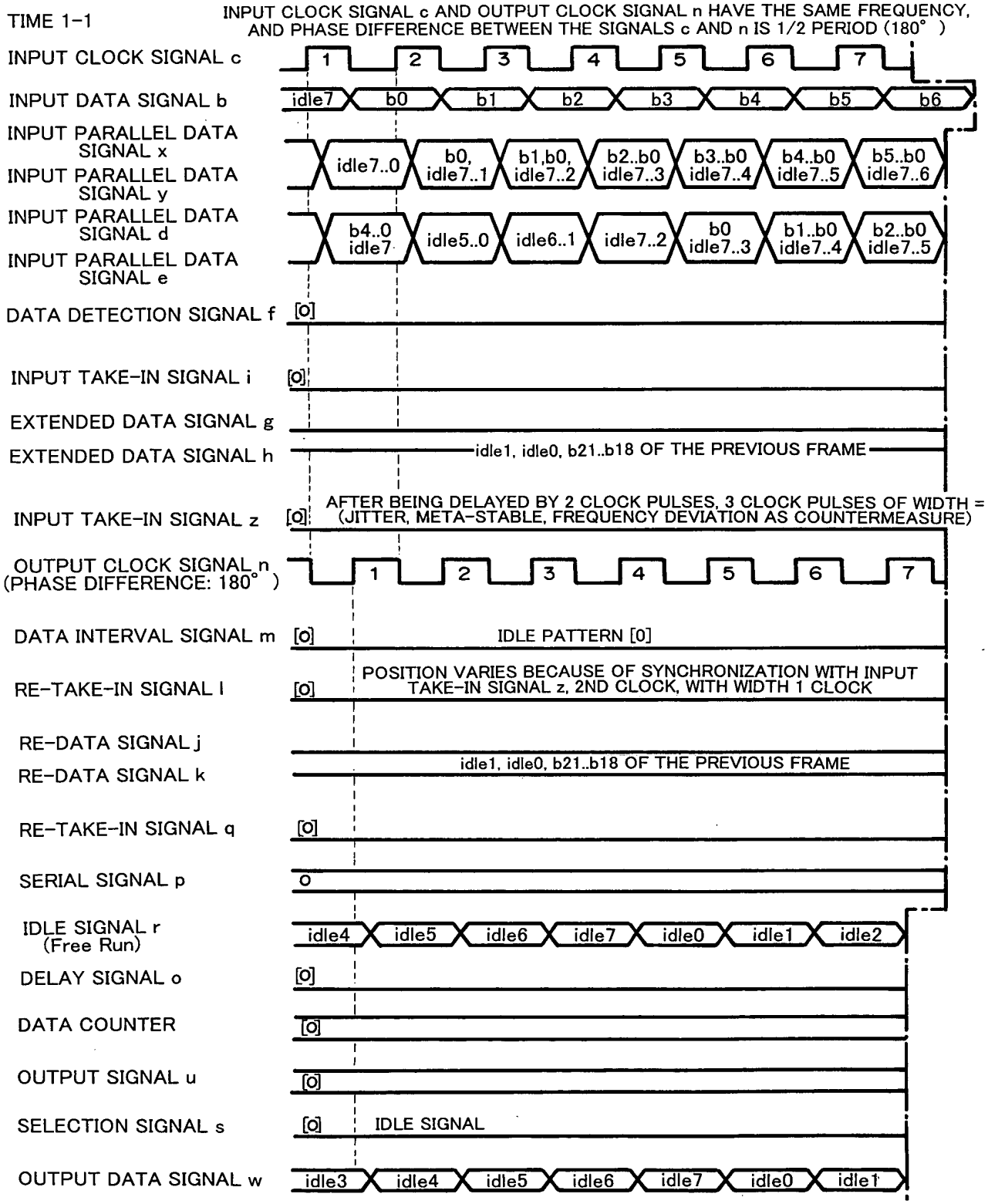

TIME 1-1
INPUT CLOCK SIGNAL n AND OUTPUT CLOCK SIGNAL n HAVE THE SAME FREQUENCY, AND PHASE DIFFERENCE BETWEEN THE SIGNALS c AND n IS 1/2 PERIOD (180°)
INPUT CLOCK SIGNAL c
1
2
3
4
5
6
7
INPUT DATA SIGNAL b
idle7
b0
b1
b2
b3
b4
b5
b6
INPUT PARALLEL DATA SIGNAL x
INPUT PARALLEL DATA SIGNAL y
INPUT PARALLEL DATA SIGNAL d
INPUT PARALLEL DATA SIGNAL e
idle7..0
b0, idle7..1
b1,b0, idle7..2
b2..b0 idle7..3
b3..b0 idle7..4
b4..b0 idle7..5
b5..b0 idle7..6
b4..0 idle7
idle5..0
idle6..1
idle7..2
b0 idle7..3
b1..b0 idle7..4
b2..b0 idle7..5
DATA DETECTION SIGNAL f
[0]
INPUT TAKE-IN SIGNAL i
EXTENDED DATA SIGNAL g
EXTENDED DATA SIGNAL h
idle1, idle0, b21..b18 OF THE PREVIOUS FRAME
INPUT TAKE-IN SIGNAL z
AFTER BEING DELAYED BY 2 CLOCK PULSES, 3 CLOCK PULSES OF WIDTH = (JITTER, META-STABLE, FREQUENCY DEVIATION AS COUNTERMEASURE)
OUTPUT CLOCK SIGNAL n (PHASE DIFFERENCE: 180°)
DATA INTERVAL SIGNAL m
IDLE PATTERN [0]
RE-TAKE-IN SIGNAL l
POSITION VARIES BECAUSE OF SYNCHRONIZATION WITH INPUT TAKE-IN SIGNAL z, 2ND CLOCK, WITH WIDTH 1 CLOCK
RE-DATA SIGNAL j
RE-DATA SIGNAL k
idle1, idle0, b21..b18 OF THE PREVIOUS FRAME
RE-TAKE-IN SIGNAL q
SERIAL SIGNAL p
o
IDLE SIGNAL r (Free Run)
idle4
idle5
idle6
idle7
idle0
idle1
idle2
DELAY SIGNAL o
DATA COUNTER
OUTPUT SIGNAL u
SELECTION SIGNAL s
IDLE SIGNAL
OUTPUT DATA SIGNAL w
idle3
idle4
idle5
idle6
idle7
idle0
idle1

FIG.2B

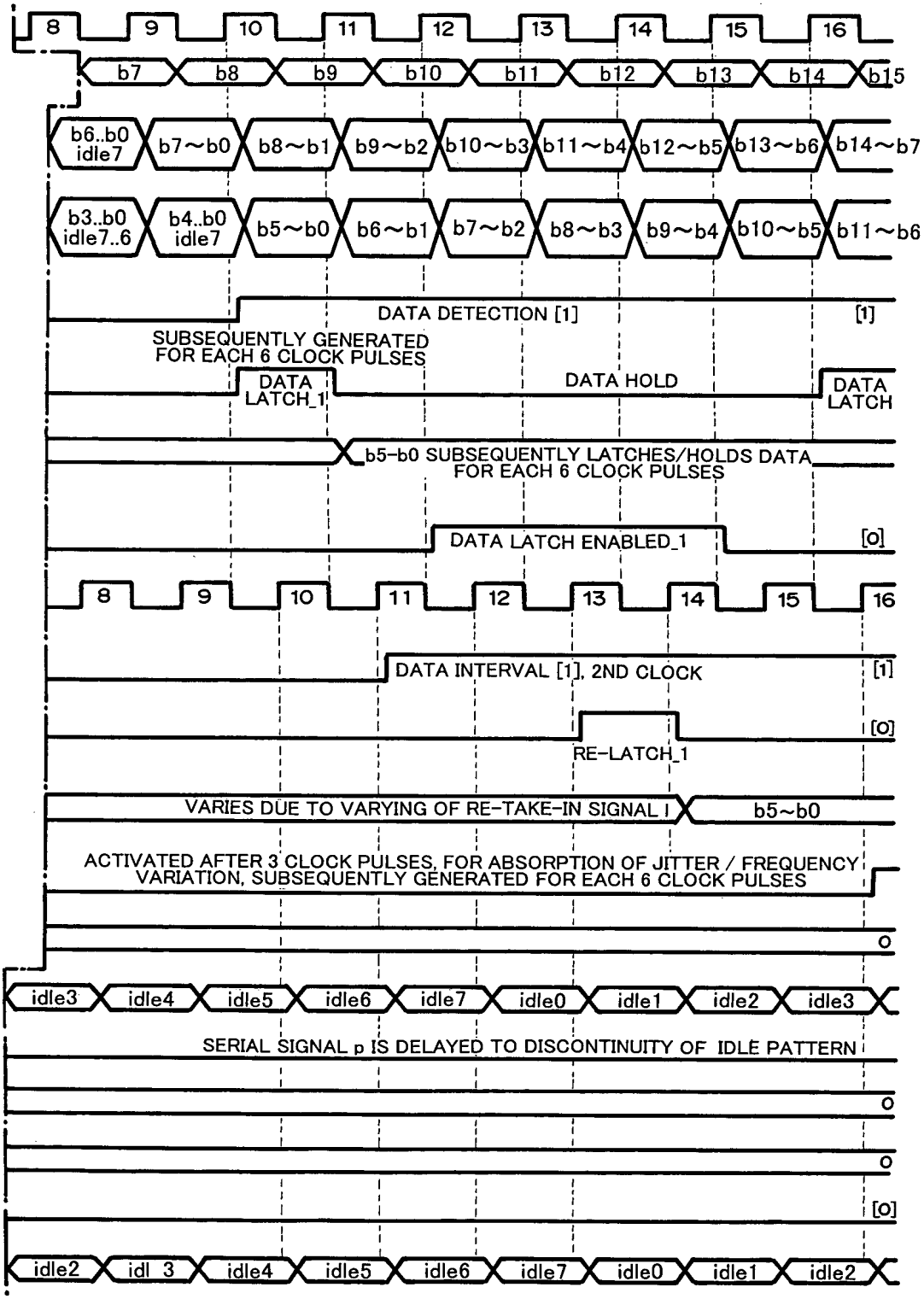

8
9
10
11
12
13
14
15
16
b7
b8
b9
b10
b11
b12
b13
b14
b15
b6..b0 idle7
b7~b0
b8~b1
b9~b2
b10~b3
b11~b4
b12~b5
b13~b6
b14~b7
b3..b0 idle7..6
b4..b0 idle7
b5~b0
b6~b1
b7~b2
b8~b3
b9~b4
b10~b5
b11~b6
DATA DETECTION [1]
[1]
SUBSEQUENTLY GENERATED FOR EACH 6 CLOCK PULSES
DATA LATCH_1
DATA HOLD
DATA LATCH
b5-b0 SUBSEQUENTLY LATCHES/HOLDS DATA FOR EACH 6 CLOCK PULSES
DATA LATCH ENABLED_1
[0]
8
9
10
11
12
13
14
15
16
DATA INTERVAL [1], 2ND CLOCK
[1]
[0]
RE-LATCH_1
VARIES DUE TO VARYING OF RE-TAKE-IN SIGNAL I
b5~b0
ACTIVATED AFTER 3 CLOCK PULSES, FOR ABSORPTION OF JITTER / FREQUENCY VARIATION, SUBSEQUENTLY GENERATED FOR EACH 6 CLOCK PULSES
0
idle3
idle4
idle5
idle6
idle7
idle0
idle1
idle2
idle3
SERIAL SIGNAL p IS DELAYED TO DISCONTINUITY OF IDLE PATTERN
0
0
[0]
idle2
idl 3
idle4
idle5
idle6
idle7
idle0
idle1
idle2

FIG.3A

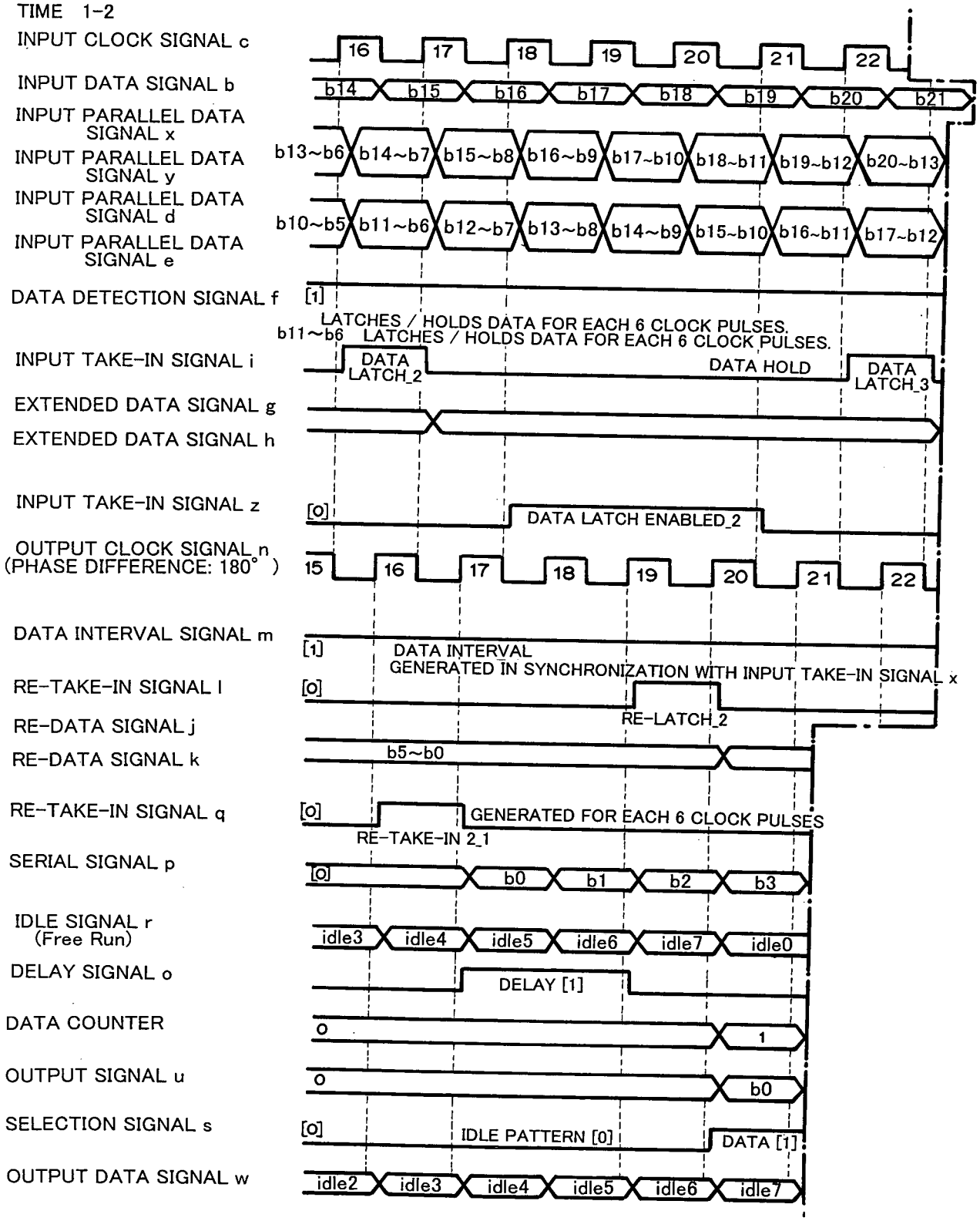

TIME 1-2
INPUT CLOCK SIGNAL c
INPUT DATA SIGNAL b
INPUT PARALLEL DATA SIGNAL x
INPUT PARALLEL DATA SIGNAL y
INPUT PARALLEL DATA SIGNAL d
INPUT PARALLEL DATA SIGNAL e
DATA DETECTION SIGNAL f
INPUT TAKE-IN SIGNAL i
EXTENDED DATA SIGNAL g
EXTENDED DATA SIGNAL h
INPUT TAKE-IN SIGNAL z
OUTPUT CLOCK SIGNAL n (PHASE DIFFERENCE: 180°)
DATA INTERVAL SIGNAL m
RE-TAKE-IN SIGNAL l
RE-DATA SIGNAL j
RE-DATA SIGNAL k
RE-TAKE-IN SIGNAL q
SERIAL SIGNAL p
IDLE SIGNAL r (Free Run)
DELAY SIGNAL o
DATA COUNTER
OUTPUT SIGNAL u
SELECTION SIGNAL s
OUTPUT DATA SIGNAL w
16 17 18 19 20 21 22
b14 b15 b16 b17 b18 b19 b20 b21
b13~b6 b14~b7 b15~b8 b16~b9 b17~b10 b18~b11 b19~b12 b20~b13
b10~b5 b11~b6 b12~b7 b13~b8 b14~b9 b15~b10 b16~b11 b17~b12
[1]
LATCHES / HOLDS DATA FOR EACH 6 CLOCK PULSES.
b11~b6 LATCHES / HOLDS DATA FOR EACH 6 CLOCK PULSES.
DATA LATCH_2
DATA HOLD
DATA LATCH_3
[0]
DATA LATCH ENABLED_2
15 16 17 18 19 20 21 22
[1]
DATA INTERVAL
GENERATED IN SYNCHRONIZATION WITH INPUT TAKE-IN SIGNAL x
[0]
RE-LATCH_2
b5~b0
[0]
GENERATED FOR EACH 6 CLOCK PULSES
RE-TAKE-IN 2_1
[0] b0 b1 b2 b3
idle3 idle4 idle5 idle6 idle7 idle0
DELAY [1]
0 1
0 b0
[0]
IDLE PATTERN [0]
DATA [1]
idle2 idle3 idle4 idle5 idle6 idle7

FIG.3B

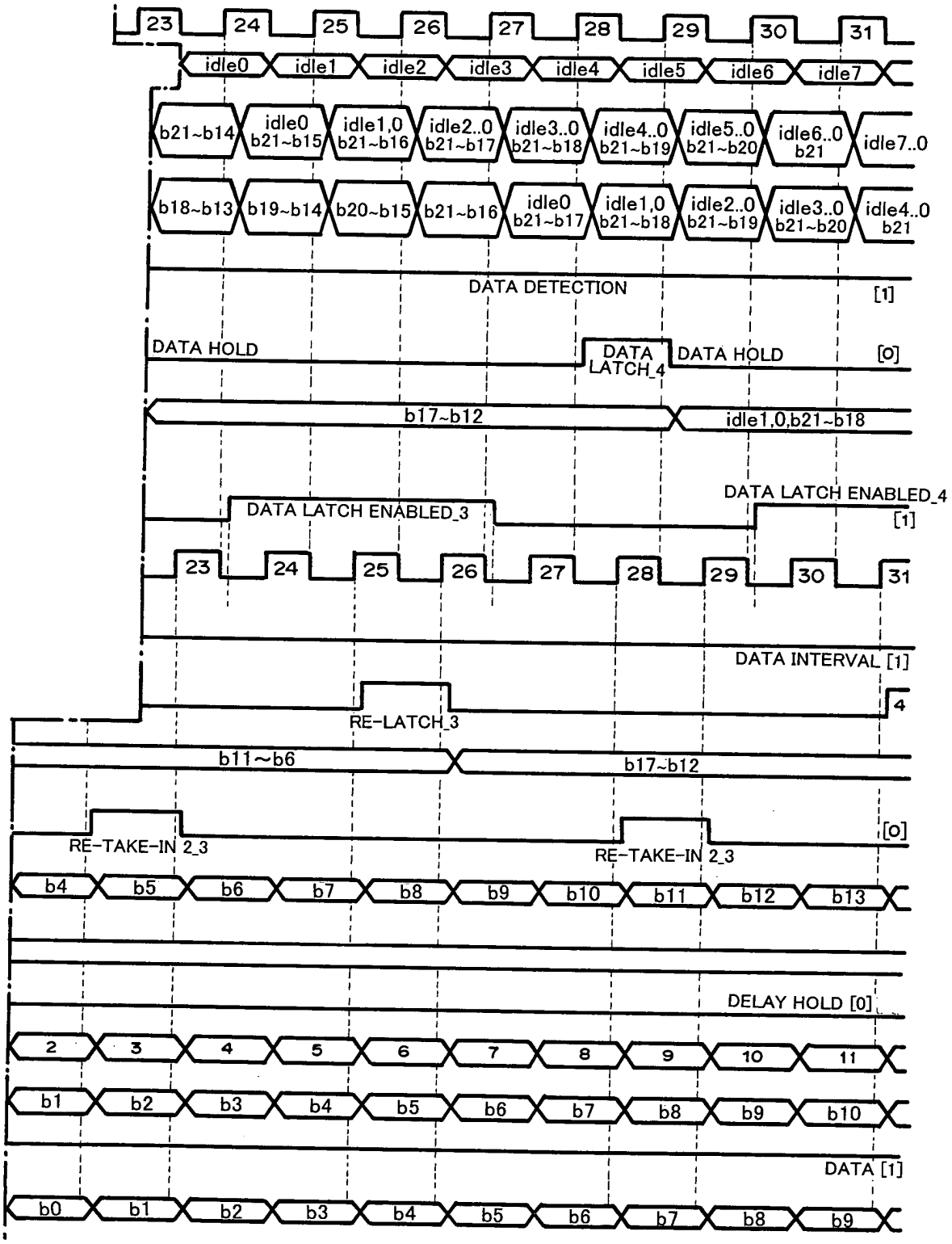

23
24
25
26
27
28
29
30
31
idle0
idle1
idle2
idle3
idle4
idle5
idle6
idle7
b21~b14
idle0 b21~b15
idle1,0 b21~b16
idle2..0 b21~b17
idle3..0 b21~b18
idle4..0 b21~b19
idle5..0 b21~b20
idle6..0 b21
idle7..0
b18~b13
b19~b14
b20~b15
b21~b16
idle0 b21~b17
idle1,0 b21~b18
idle2..0 b21~b19
idle3..0 b21~b20
idle4..0 b21
DATA DETECTION
[1]
DATA HOLD
DATA LATCH_4
DATA HOLD
[0]
b17~b12
idle1,0,b21~b18
DATA LATCH ENABLED_3
DATA LATCH ENABLED_4
[1]
23
24
25
26
27
28
29
30
31
DATA INTERVAL [1]
RE-LATCH_3
4
b11~b6
b17~b12
RE-TAKE-IN 2_3
RE-TAKE-IN 2_3
[0]
b4
b5
b6
b7
b8
b9
b10
b11
b12
b13
DELAY HOLD [0]
2
3
4
5
6
7
8
9
10
11
b1
b2
b3
b4
b5
b6
b7
b8
b9
b10
DATA [1]
b0
b1
b2
b3
b4
b5
b6
b7
b8
b9

FIG.4A

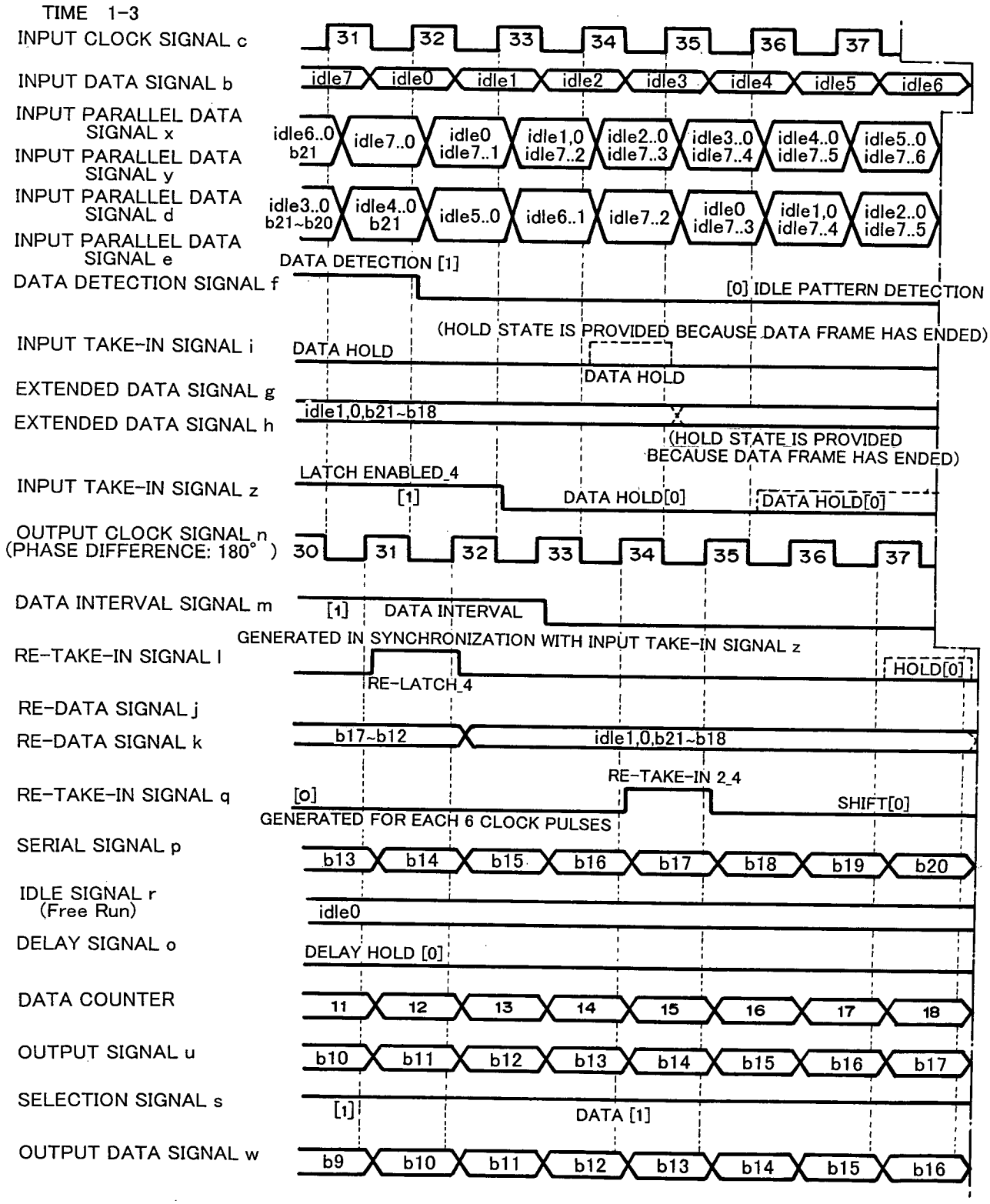

TIME 1-3
INPUT CLOCK SIGNAL c
31
32
33
34
35
36
37
INPUT DATA SIGNAL b
idle7
idle0
idle1
idle2
idle3
idle4
idle5
idle6
INPUT PARALLEL DATA SIGNAL x
idle6..0 b21
idle7..0
idle0 idle7..1
idle1,0 idle7..2
idle2..0 idle7..3
idle3..0 idle7..4
idle4..0 idle7..5
idle5..0 idle7..6
INPUT PARALLEL DATA SIGNAL y
INPUT PARALLEL DATA SIGNAL d
idle3..0 b21~b20
idle4..0 b21
idle5..0
idle6..1
idle7..2
idle0 idle7..3
idle1,0 idle7..4
idle2..0 idle7..5
INPUT PARALLEL DATA SIGNAL e
DATA DETECTION [1]
DATA DETECTION SIGNAL f
[0] IDLE PATTERN DETECTION
(HOLD STATE IS PROVIDED BECAUSE DATA FRAME HAS ENDED)
INPUT TAKE-IN SIGNAL i
DATA HOLD
DATA HOLD
EXTENDED DATA SIGNAL g
idle1,0,b21~b18
EXTENDED DATA SIGNAL h
(HOLD STATE IS PROVIDED BECAUSE DATA FRAME HAS ENDED)
LATCH ENABLED_4
INPUT TAKE-IN SIGNAL z
[1]
DATA HOLD[0]
DATA HOLD[0]
OUTPUT CLOCK SIGNAL n (PHASE DIFFERENCE: 180°)
30
31
32
33
34
35
36
37
DATA INTERVAL SIGNAL m
[1]
DATA INTERVAL
GENERATED IN SYNCHRONIZATION WITH INPUT TAKE-IN SIGNAL z
RE-TAKE-IN SIGNAL l
RE-LATCH_4
HOLD[0]
RE-DATA SIGNAL j
RE-DATA SIGNAL k
b17~b12
idle1,0,b21~b18
RE-TAKE-IN 2_4
RE-TAKE-IN SIGNAL q
[0]
SHIFT[0]
GENERATED FOR EACH 6 CLOCK PULSES
SERIAL SIGNAL p
b13
b14
b15
b16
b17
b18
b19
b20
IDLE SIGNAL r (Free Run)
idle0
DELAY SIGNAL o
DELAY HOLD [0]
DATA COUNTER
11
12
13
14
15
16
17
18
OUTPUT SIGNAL u
b10
b11
b12
b13
b14
b15
b16
b17
SELECTION SIGNAL s
[1]
DATA [1]
OUTPUT DATA SIGNAL w
b9
b10
b11
b12
b13
b14
b15
b16

FIG.4B

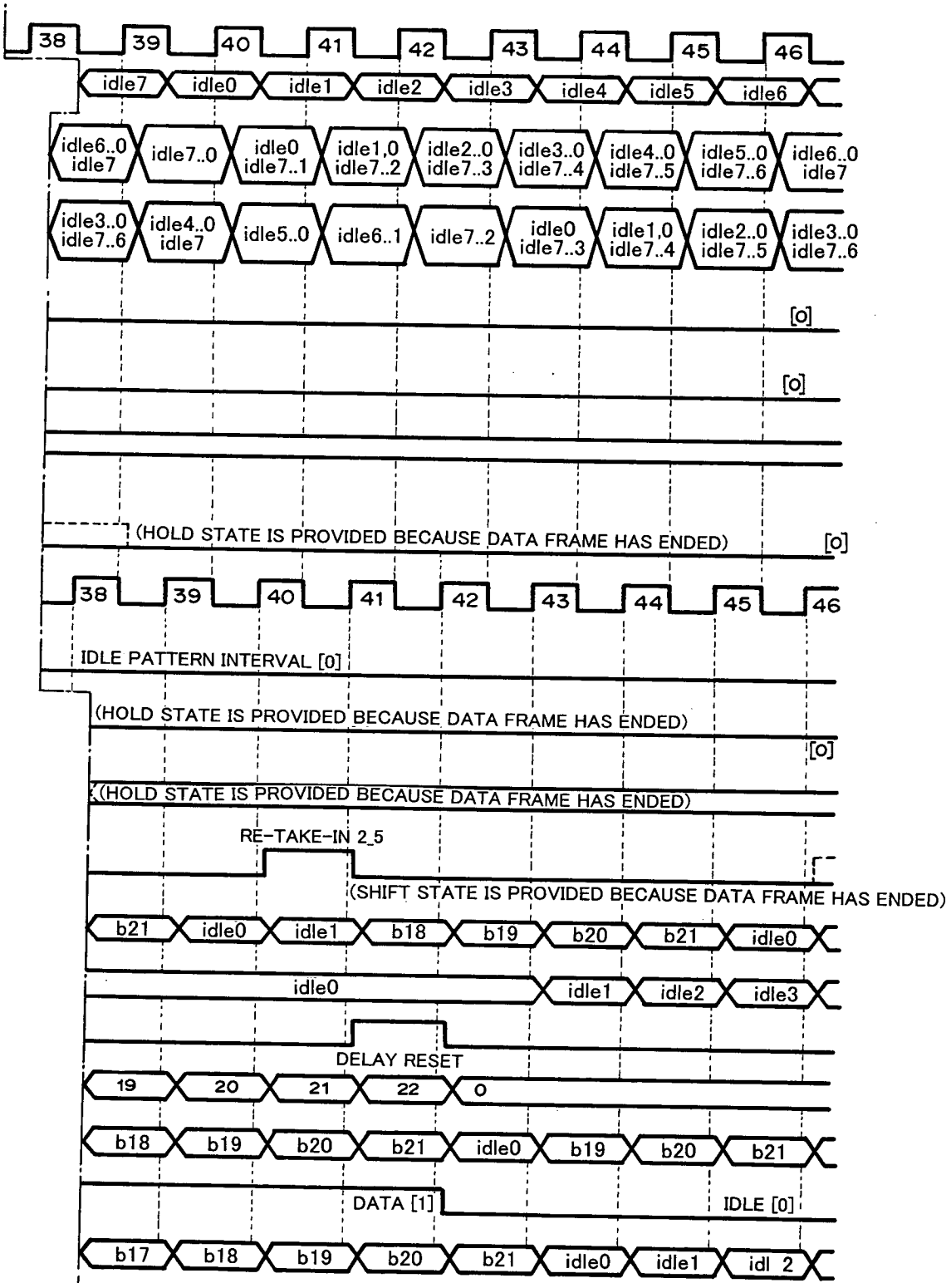

38
39
40
41
42
43
44
45
46
idle7
idle0
idle1
idle2
idle3
idle4
idle5
idle6
idle6..0 idle7
idle7..0
idle0 idle7..1
idle1,0 idle7..2
idle2..0 idle7..3
idle3..0 idle7..4
idle4..0 idle7..5
idle5..0 idle7..6
idle6..0 idle7
idle3..0 idle7..6
idle4..0 idle7
idle5..0
idle6..1
idle7..2
idle0 idle7..3
idle1,0 idle7..4
idle2..0 idle7..5
idle3..0 idle7..6
[o]
[o]
(HOLD STATE IS PROVIDED BECAUSE DATA FRAME HAS ENDED)
[o]
38
39
40
41
42
43
44
45
46
IDLE PATTERN INTERVAL [0]
(HOLD STATE IS PROVIDED BECAUSE DATA FRAME HAS ENDED)
[o]
(HOLD STATE IS PROVIDED BECAUSE DATA FRAME HAS ENDED)
RE-TAKE-IN 2_5
(SHIFT STATE IS PROVIDED BECAUSE DATA FRAME HAS ENDED)
b21
idle0
idle1
b18
b19
b20
b21
idle0
idle0
idle1
idle2
idle3
DELAY RESET
19
20
21
22
0
b18
b19
b20
b21
idle0
b19
b20
b21
DATA [1]
IDLE [0]
b17
b18
b19
b20
b21
idle0
idle1
idl 2

FIG.5A

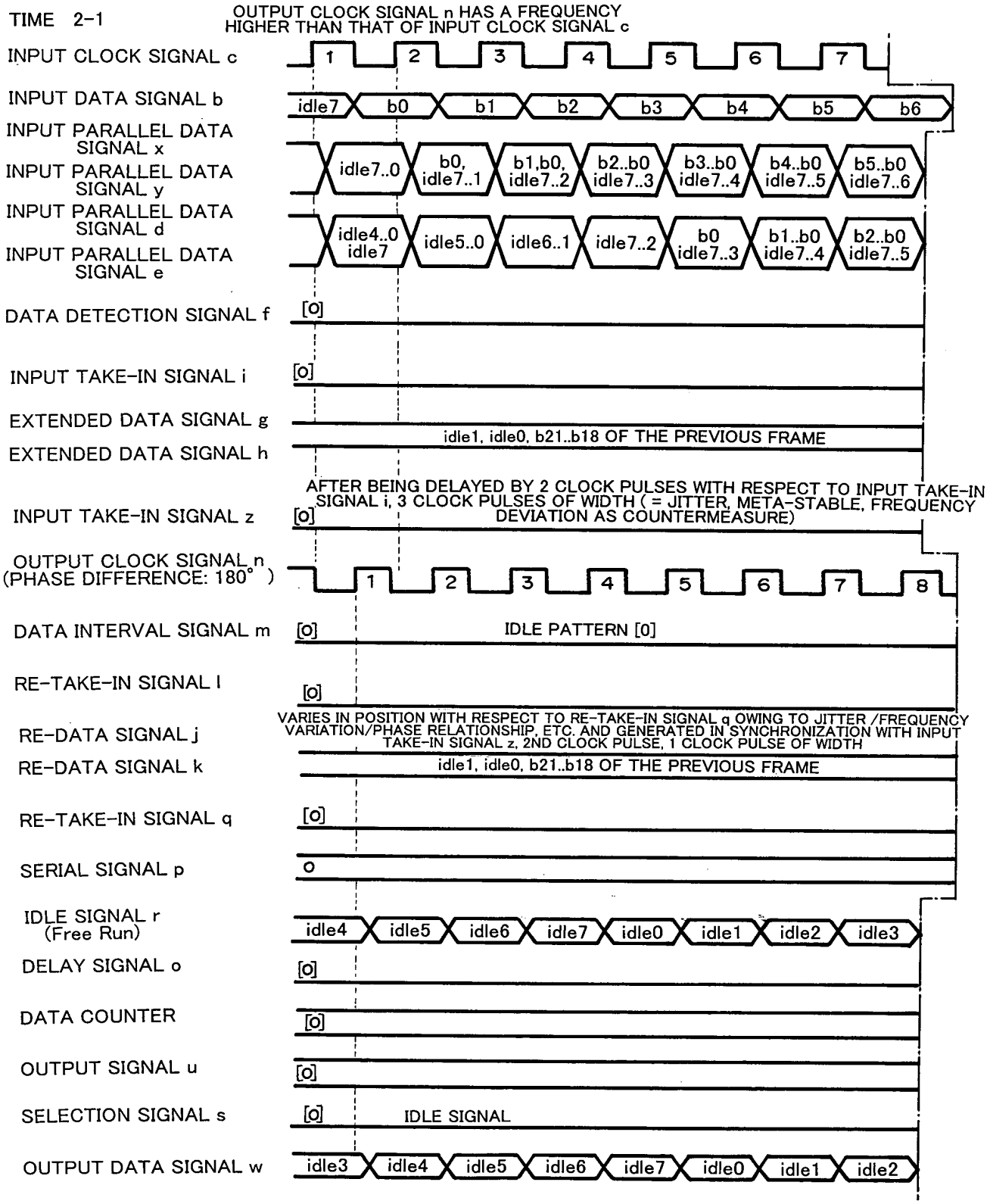

TIME 2-1
OUTPUT CLOCK SIGNAL n HAS A FREQUENCY HIGHER THAN THAT OF INPUT CLOCK SIGNAL c
INPUT CLOCK SIGNAL c
1
2
3
4
5
6
7
INPUT DATA SIGNAL b
idle7
b0
b1
b2
b3
b4
b5
b6
INPUT PARALLEL DATA SIGNAL x
INPUT PARALLEL DATA SIGNAL y
idle7..0
b0, idle7..1
b1,b0, idle7..2
b2..b0 idle7..3
b3..b0 idle7..4
b4..b0 idle7..5
b5..b0 idle7..6
INPUT PARALLEL DATA SIGNAL d
INPUT PARALLEL DATA SIGNAL e
idle4..0 idle7
idle5..0
idle6..1
idle7..2
b0 idle7..3
b1..b0 idle7..4
b2..b0 idle7..5
DATA DETECTION SIGNAL f
[0]
INPUT TAKE-IN SIGNAL i
[0]
EXTENDED DATA SIGNAL g
idle1, idle0, b21..b18 OF THE PREVIOUS FRAME
EXTENDED DATA SIGNAL h
AFTER BEING DELAYED BY 2 CLOCK PULSES WITH RESPECT TO INPUT TAKE-IN SIGNAL i, 3 CLOCK PULSES OF WIDTH (= JITTER, META-STABLE, FREQUENCY DEVIATION AS COUNTERMEASURE)
INPUT TAKE-IN SIGNAL z
[0]
OUTPUT CLOCK SIGNAL n (PHASE DIFFERENCE: 180°)
1
2
3
4
5
6
7
8
DATA INTERVAL SIGNAL m
[0]
IDLE PATTERN [0]
RE-TAKE-IN SIGNAL l
[0]
VARIES IN POSITION WITH RESPECT TO RE-TAKE-IN SIGNAL q OWING TO JITTER /FREQUENCY VARIATION/PHASE RELATIONSHIP, ETC. AND GENERATED IN SYNCHRONIZATION WITH INPUT TAKE-IN SIGNAL z, 2ND CLOCK PULSE, 1 CLOCK PULSE OF WIDTH
RE-DATA SIGNAL j
RE-DATA SIGNAL k
idle1, idle0, b21..b18 OF THE PREVIOUS FRAME
RE-TAKE-IN SIGNAL q
[0]
SERIAL SIGNAL p
0
IDLE SIGNAL r (Free Run)
idle4
idle5
idle6
idle7
idle0
idle1
idle2
idle3
DELAY SIGNAL o
[0]
DATA COUNTER
[0]
OUTPUT SIGNAL u
[0]
SELECTION SIGNAL s
[0]
IDLE SIGNAL
OUTPUT DATA SIGNAL w
idle3
idle4
idle5
idle6
idle7
idle0
idle1
idle2

FIG.5B

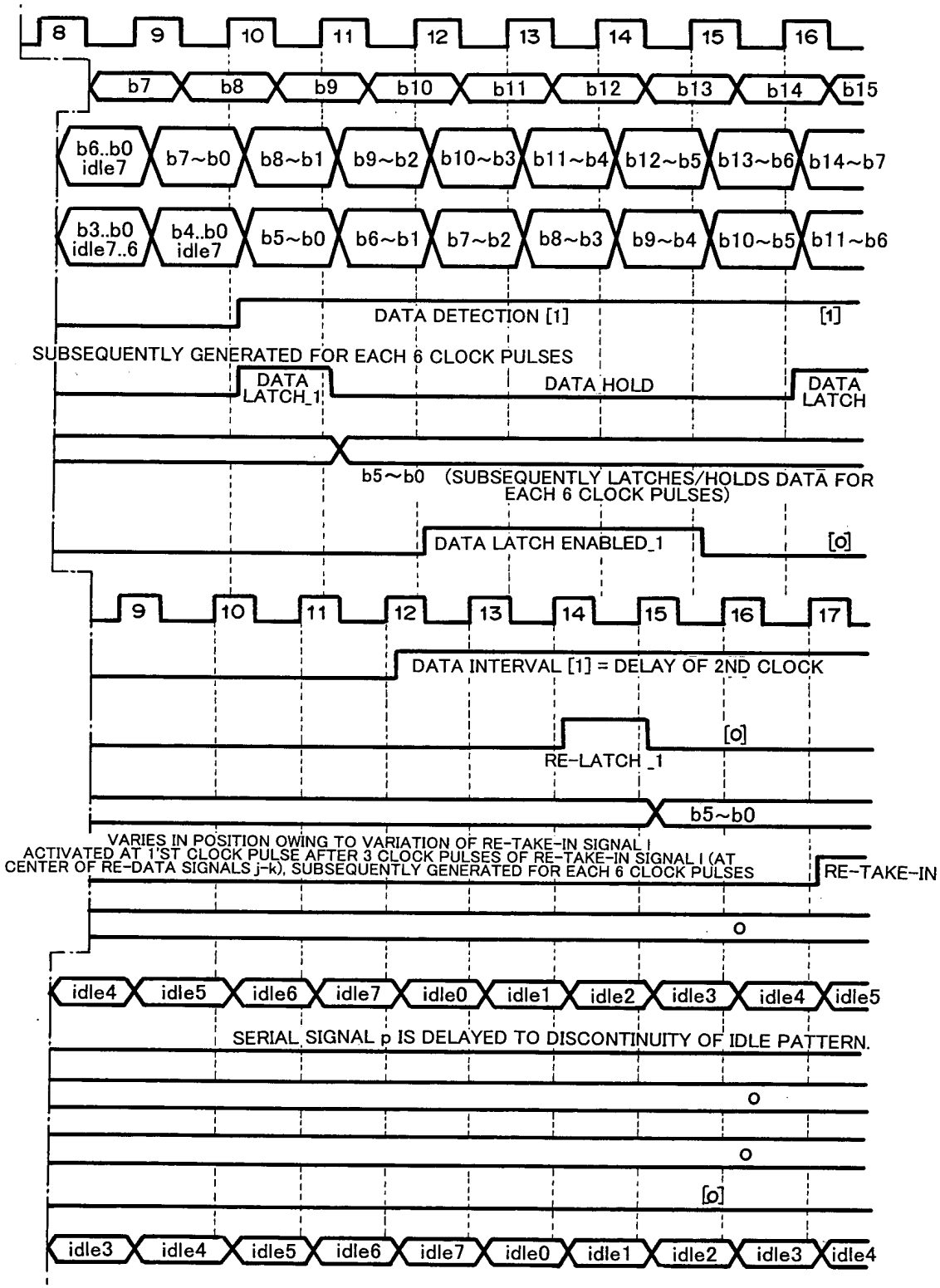

8
9
10
11
12
13
14
15
16
b7
b8
b9
b10
b11
b12
b13
b14
b15
b6..b0 idle7
b7~b0
b8~b1
b9~b2
b10~b3
b11~b4
b12~b5
b13~b6
b14~b7
b3..b0 idle7..6
b4..b0 idle7
b5~b0
b6~b1
b7~b2
b8~b3
b9~b4
b10~b5
b11~b6
DATA DETECTION [1]
[1]
SUBSEQUENTLY GENERATED FOR EACH 6 CLOCK PULSES
DATA LATCH_1
DATA HOLD
DATA LATCH
b5~b0 (SUBSEQUENTLY LATCHES/HOLDS DATA FOR EACH 6 CLOCK PULSES)
DATA LATCH ENABLED_1
[0]
9
10
11
12
13
14
15
16
17
DATA INTERVAL [1] = DELAY OF 2ND CLOCK
[0]
RE-LATCH _1
b5~b0
VARIES IN POSITION OWING TO VARIATION OF RE-TAKE-IN SIGNAL I
ACTIVATED AT 1'ST CLOCK PULSE AFTER 3 CLOCK PULSES OF RE-TAKE-IN SIGNAL I (AT CENTER OF RE-DATA SIGNALS j-k), SUBSEQUENTLY GENERATED FOR EACH 6 CLOCK PULSES
RE-TAKE-IN
o
idle4
idle5
idle6
idle7
idle0
idle1
idle2
idle3
idle4
idle5
SERIAL SIGNAL p IS DELAYED TO DISCONTINUITY OF IDLE PATTERN.
o
o
[0]
idle3
idle4
idle5
idle6
idle7
idle0
idle1
idle2
idle3
idle4

FIG.6A

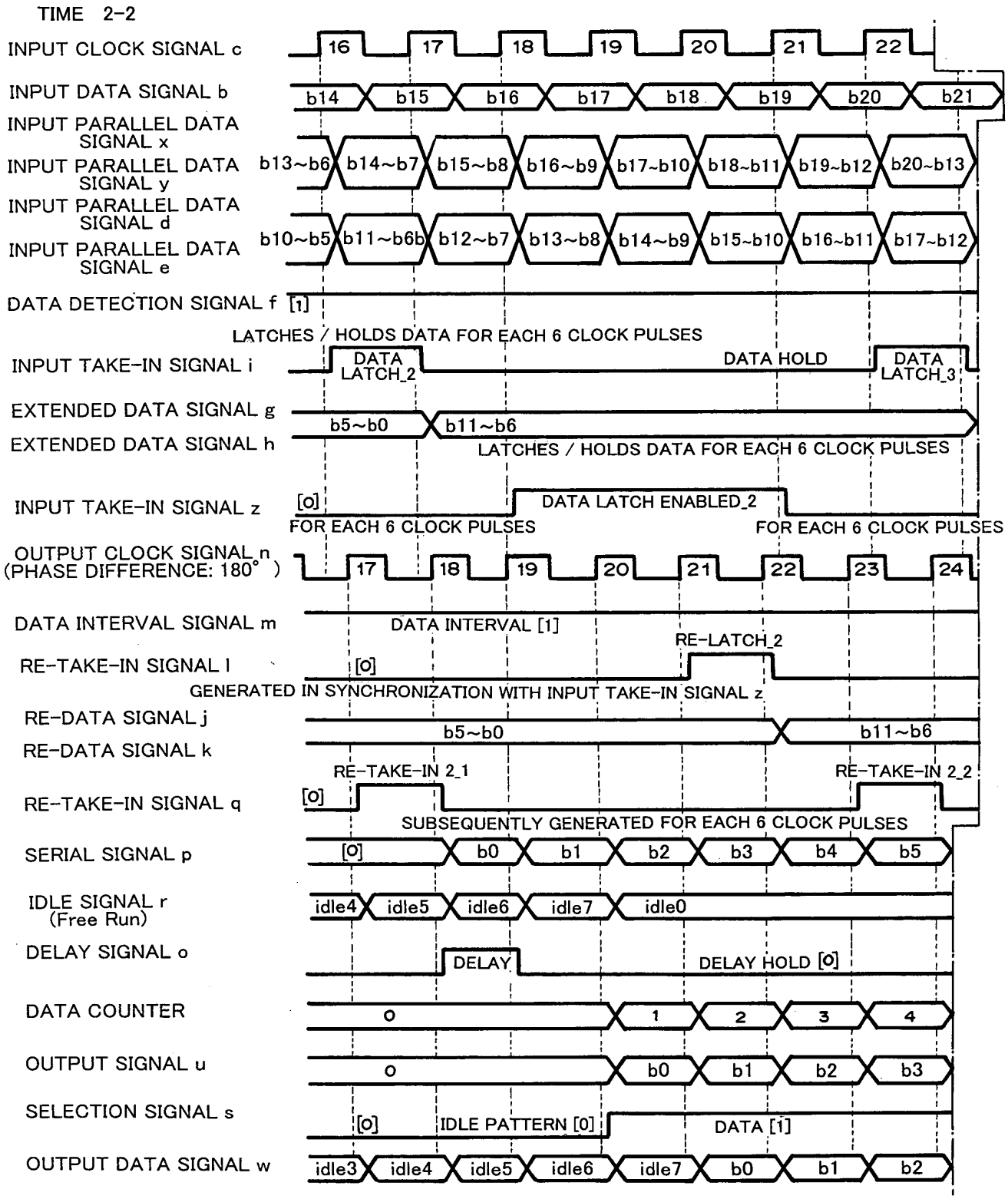

TIME 2-2
INPUT CLOCK SIGNAL c
16
17
18
19
20
21
22
INPUT DATA SIGNAL b
b14
b15
b16
b17
b18
b19
b20
b21
INPUT PARALLEL DATA SIGNAL x
INPUT PARALLEL DATA SIGNAL y
b13~b6
b14~b7
b15~b8
b16~b9
b17~b10
b18~b11
b19~b12
b20~b13
INPUT PARALLEL DATA SIGNAL d
INPUT PARALLEL DATA SIGNAL e
b10~b5
b11~b6b
b12~b7
b13~b8
b14~b9
b15~b10
b16~b11
b17~b12
DATA DETECTION SIGNAL f
[1]
LATCHES / HOLDS DATA FOR EACH 6 CLOCK PULSES
INPUT TAKE-IN SIGNAL i
DATA LATCH_2
DATA HOLD
DATA LATCH_3
EXTENDED DATA SIGNAL g
EXTENDED DATA SIGNAL h
b5~b0
b11~b6
LATCHES / HOLDS DATA FOR EACH 6 CLOCK PULSES
INPUT TAKE-IN SIGNAL z
[0]
DATA LATCH ENABLED_2
FOR EACH 6 CLOCK PULSES
FOR EACH 6 CLOCK PULSES
OUTPUT CLOCK SIGNAL n (PHASE DIFFERENCE: 180°)
17
18
19
20
21
22
23
24
DATA INTERVAL SIGNAL m
DATA INTERVAL [1]
RE-TAKE-IN SIGNAL l
RE-LATCH_2
[0]
GENERATED IN SYNCHRONIZATION WITH INPUT TAKE-IN SIGNAL z
RE-DATA SIGNAL j
RE-DATA SIGNAL k
b5~b0
b11~b6
RE-TAKE-IN SIGNAL q
RE-TAKE-IN 2_1
RE-TAKE-IN 2_2
[0]
SUBSEQUENTLY GENERATED FOR EACH 6 CLOCK PULSES
SERIAL SIGNAL p
[0]
b0
b1
b2
b3
b4
b5
IDLE SIGNAL r (Free Run)
idle4
idle5
idle6
idle7
idle0
DELAY SIGNAL o
DELAY
DELAY HOLD [0]
DATA COUNTER
0
1
2
3
4
OUTPUT SIGNAL u
0
b0
b1
b2
b3
SELECTION SIGNAL s
[0]
IDLE PATTERN [0]
DATA [1]
OUTPUT DATA SIGNAL w
idle3
idle4
idle5
idle6
idle7
b0
b1
b2

FIG.6B

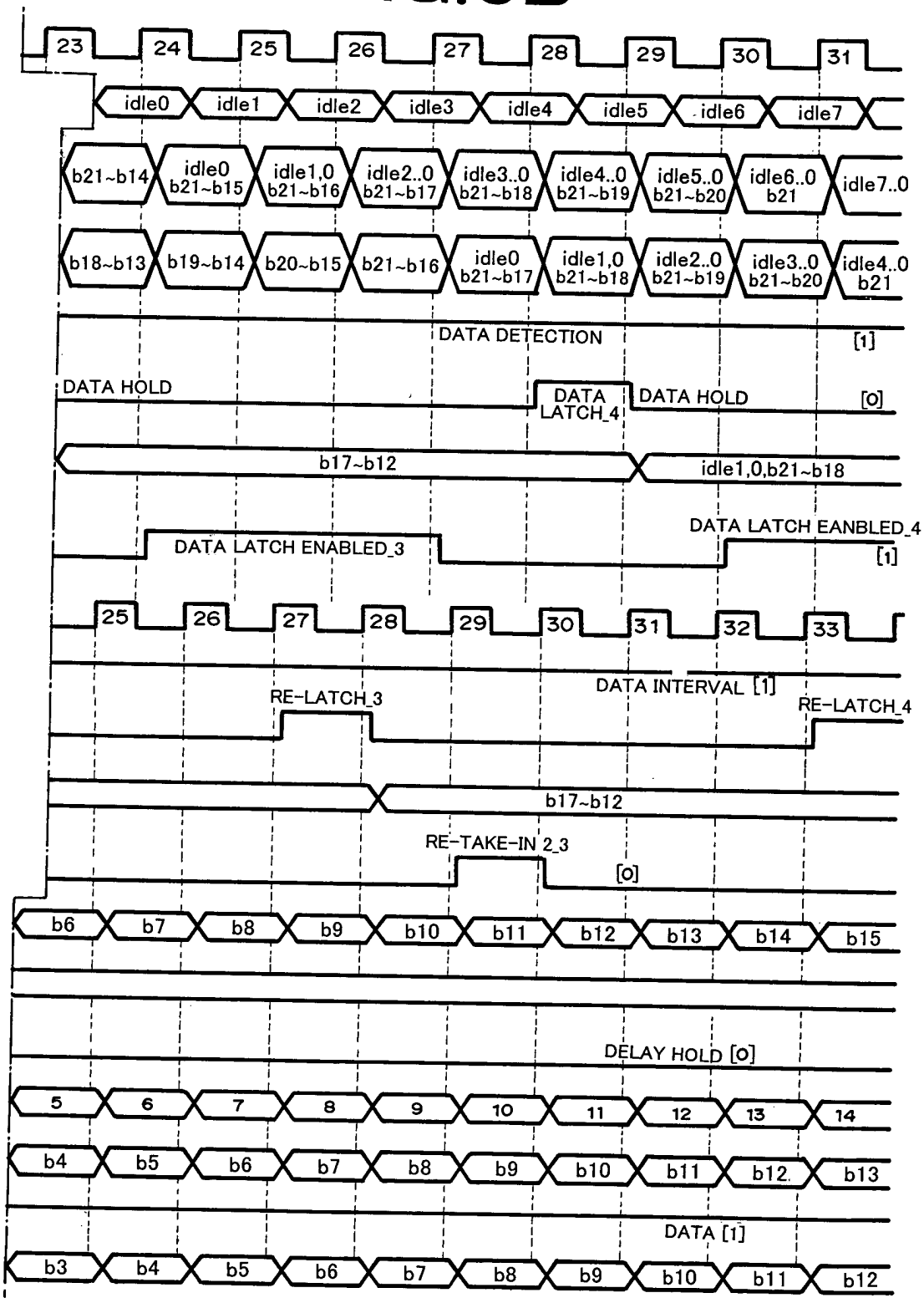

23
24
25
26
27
28
29
30
31
idle0
idle1
idle2
idle3
idle4
idle5
idle6
idle7
b21~b14
idle0 b21~b15
idle1,0 b21~b16
idle2..0 b21~b17
idle3..0 b21~b18
idle4..0 b21~b19
idle5..0 b21~b20
idle6..0 b21
idle7..0
b18~b13
b19~b14
b20~b15
b21~b16
idle0 b21~b17
idle1,0 b21~b18
idle2..0 b21~b19
idle3..0 b21~b20
idle4..0 b21
DATA DETECTION
[1]
DATA HOLD
DATA LATCH_4
DATA HOLD
[0]
b17~b12
idle1,0,b21~b18
DATA LATCH ENABLED_3
DATA LATCH EANBLED_4
[1]
25
26
27
28
29
30
31
32
33
DATA INTERVAL [1]
RE-LATCH_3
RE-LATCH_4
b17~b12
RE-TAKE-IN 2_3
[0]
b6
b7
b8
b9
b10
b11
b12
b13
b14
b15
DELAY HOLD [0]
5
6
7
8
9
10
11
12
13
14
b4
b5
b6
b7
b8
b9
b10
b11
b12
b13
DATA [1]
b3
b4
b5
b6
b7
b8
b9
b10
b11
b12

FIG.7A

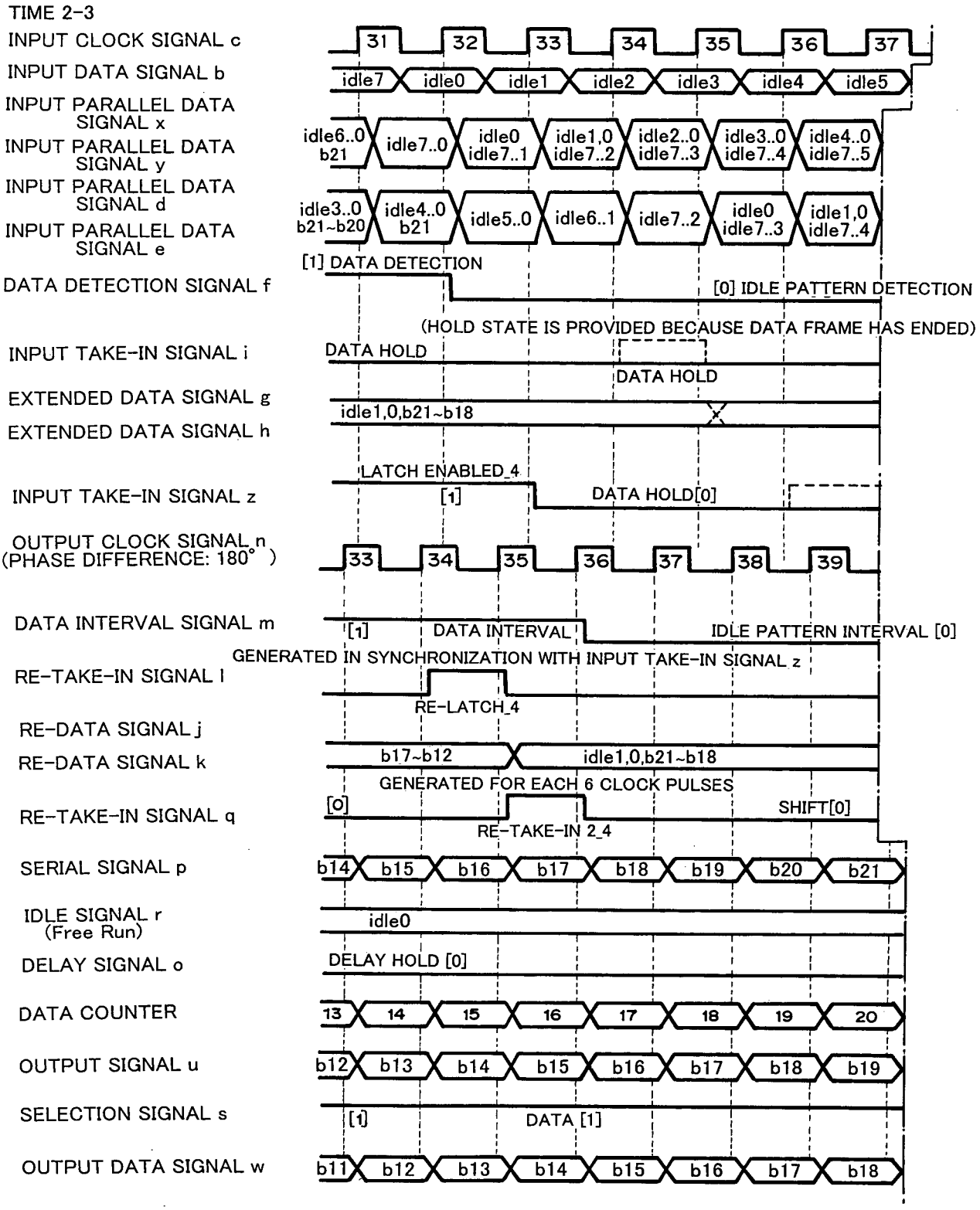
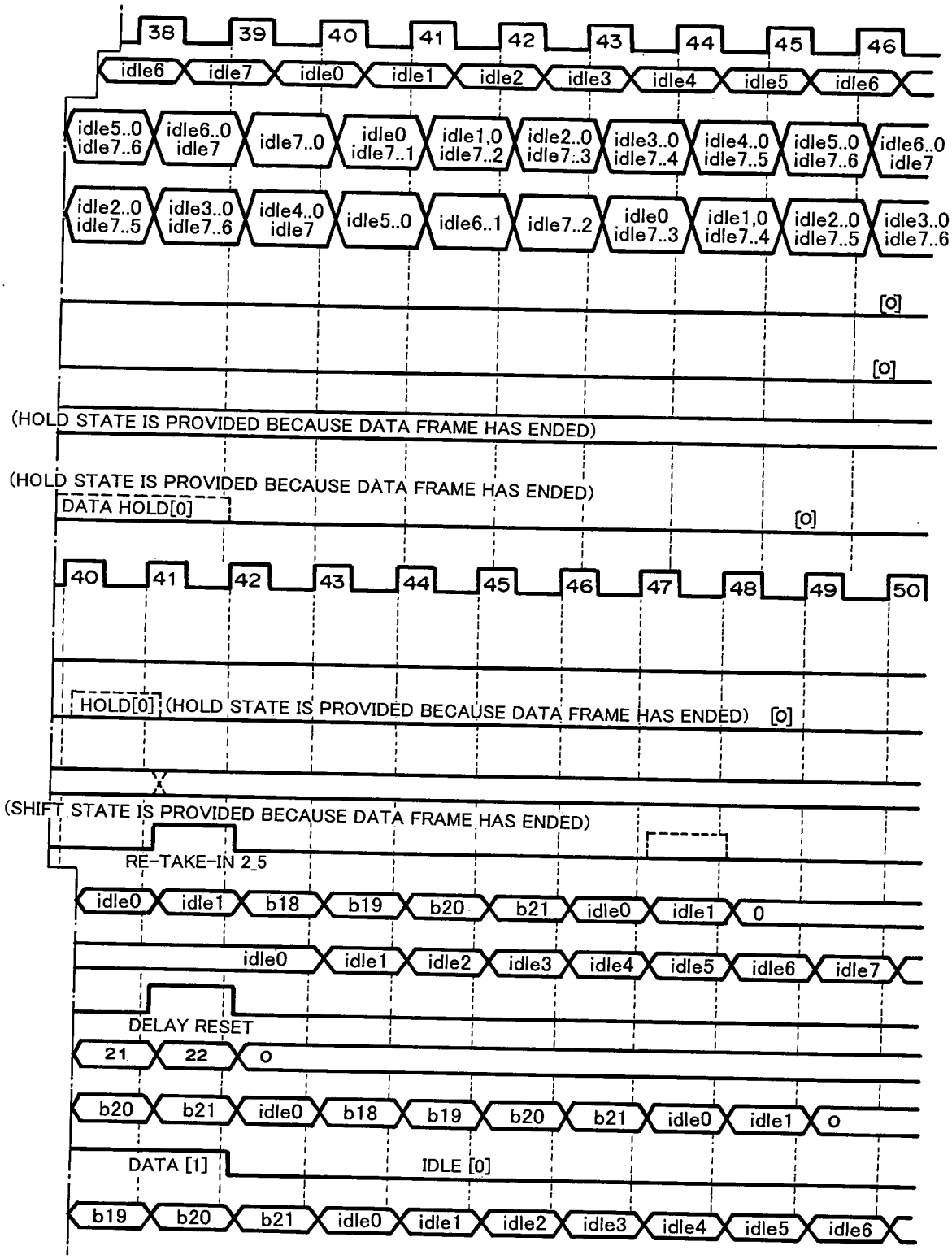

TIME 2-3
INPUT CLOCK SIGNAL c
INPUT DATA SIGNAL b
INPUT PARALLEL DATA SIGNAL x
INPUT PARALLEL DATA SIGNAL y
INPUT PARALLEL DATA SIGNAL d
INPUT PARALLEL DATA SIGNAL e
DATA DETECTION SIGNAL f
INPUT TAKE-IN SIGNAL i
EXTENDED DATA SIGNAL g
EXTENDED DATA SIGNAL h
INPUT TAKE-IN SIGNAL z
OUTPUT CLOCK SIGNAL n (PHASE DIFFERENCE: 180°)
DATA INTERVAL SIGNAL m
RE-TAKE-IN SIGNAL l
RE-DATA SIGNAL j
RE-DATA SIGNAL k
RE-TAKE-IN SIGNAL q
SERIAL SIGNAL p
IDLE SIGNAL r (Free Run)
DELAY SIGNAL o
DATA COUNTER
OUTPUT SIGNAL u
SELECTION SIGNAL s
OUTPUT DATA SIGNAL w
31
32
33
34
35
36
37
idle7
idle0
idle1
idle2
idle3
idle4
idle5
idle6..0 b21
idle7..0
idle0 idle7..1
idle1,0 idle7..2
idle2..0 idle7..3
idle3..0 idle7..4
idle4..0 idle7..5
idle3..0 b21~b20
idle4..0 b21
idle5..0
idle6..1
idle7..2
idle0 idle7..3
idle1,0 idle7..4
[1] DATA DETECTION
[0] IDLE PATTERN DETECTION
(HOLD STATE IS PROVIDED BECAUSE DATA FRAME HAS ENDED)
DATA HOLD
DATA HOLD
idle1,0,b21~b18
LATCH ENABLED_4
[1]
DATA HOLD[0]
33
34
35
36
37
38
39
[1]
DATA INTERVAL
IDLE PATTERN INTERVAL [0]
GENERATED IN SYNCHRONIZATION WITH INPUT TAKE-IN SIGNAL z
RE-LATCH_4
b17~b12
idle1,0,b21~b18
GENERATED FOR EACH 6 CLOCK PULSES
[0]
SHIFT[0]
RE-TAKE-IN 2_4
b14
b15
b16
b17
b18
b19
b20
b21
idle0
DELAY HOLD [0]
13
14
15
16
17
18
19
20
b12
b13
b14
b15
b16
b17
b18
b19
[1]
DATA [1]
b11
b12
b13
b14
b15
b16
b17
b18

FIG.7B


38
39
40
41
42
43
44
45
46
idle6
idle7
idle0
idle1
idle2
idle3
idle4
idle5
idle6
idle5..0 idle7..6
idle6..0 idle7
idle7..0
idle0 idle7..1
idle1,0 idle7..2
idle2..0 idle7..3
idle3..0 idle7..4
idle4..0 idle7..5
idle5..0 idle7..6
idle6..0 idle7
idle2..0 idle7..5
idle3..0 idle7..6
idle4..0 idle7
idle5..0
idle6..1
idle7..2
idle0 idle7..3
idle1,0 idle7..4
idle2..0 idle7..5
idle3..0 idle7..6
[0]
[0]
(HOLD STATE IS PROVIDED BECAUSE DATA FRAME HAS ENDED)
(HOLD STATE IS PROVIDED BECAUSE DATA FRAME HAS ENDED)
DATA HOLD[0]
[0]
40
41
42
43
44
45
46
47
48
49
50
HOLD[0]
(HOLD STATE IS PROVIDED BECAUSE DATA FRAME HAS ENDED)
[0]
(SHIFT STATE IS PROVIDED BECAUSE DATA FRAME HAS ENDED)
RE-TAKE-IN 2_5
idle0
idle1
b18
b19
b20
b21
idle0
idle1
0
idle0
idle1
idle2
idle3
idle4
idle5
idle6
idle7
DELAY RESET
21
22
0
b20
b21
idle0
b18
b19
b20
b21
idle0
idle1
0
DATA [1]
IDLE [0]
b19
b20
b21
idle0
idle1
idle2
idle3
idle4
idle5
idle6